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Terms	Documents
metallization and liners and voltage and (surface near2 potentials)	4

Database:

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L1 metallization and liners and voltage and (surface near2 potentials)**Hit Count Set Name**

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WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 4 of 4 returned.**☐ 1. Document ID: US 6143593 A

L1: Entry 1 of 4

File: USPT

Nov 7, 2000

US-PAT-NO: 6143593

DOCUMENT-IDENTIFIER: US 6143593 A

TITLE: Elevated channel MOSFET

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw. Desc	Image										

☐ 2. Document ID: US 5834371 A

L1: Entry 2 of 4

File: USPT

Nov 10, 1998

US-PAT-NO: 5834371

DOCUMENT-IDENTIFIER: US 5834371 A

TITLE: Method and apparatus for preparing and metallizing high aspect ratio silicon semiconductor device contacts to reduce the resistivity thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 3. Document ID: US 3681667 A

L1: Entry 3 of 4

File: USPT

Aug 1, 1972

US-PAT-NO: 3681667

DOCUMENT-IDENTIFIER: US 3681667 A

TITLE: CONTROLLED RECTIFIER AND TRIAC WITH Laterally OFF-SET GATE AND AUXILIARY SEGMENTS FOR ACCELERATED TURN ON

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 4. Document ID: US 3586932 A

L1: Entry 4 of 4

File: USPT

Jun 22, 1971

US-PAT-NO: 3586932

DOCUMENT-IDENTIFIER: US 3586932 A

TITLE: FIVE LAYER GATE CONTROLLED THYRISTOR WITH NOVEL TURN ON
CHARACTERISTICS

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	K00C
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WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 3 of 3 returned.**☐ 1. Document ID: US 6143593 A

L3: Entry 1 of 3

File: USPT

Nov 7, 2000

US-PAT-NO: 6143593

DOCUMENT-IDENTIFIER: US 6143593 A

TITLE: Elevated channel MOSFET

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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[KWIC](#)☐ 2. Document ID: US 6054013 A

L3: Entry 2 of 3

File: USPT

Apr 25, 2000

US-PAT-NO: 6054013

DOCUMENT-IDENTIFIER: US 6054013 A

TITLE: Parallel plate electrode plasma reactor having an inductive antenna and adjustable radial distribution of plasma ion density

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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[KWIC](#)☐ 3. Document ID: US 6036878 A

L3: Entry 3 of 3

File: USPT

Mar 14, 2000

US-PAT-NO: 6036878

DOCUMENT-IDENTIFIER: US 6036878 A

TITLE: Low density high frequency process for a parallel-plate electrode plasma reactor having an inductive antenna

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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Terms	Documents
L2 and (germanium and undoped and doped and nitride)	3

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<u>L3</u>	L2 and (germanium and undoped and doped and nitride)	3	<u>L3</u>
<u>L2</u>	(plugs or vias or interconnects or holes) and liners and voltage and (surface near2 potentials)	99	<u>L2</u>
<u>L1</u>	metallization and liners and voltage and (surface near2 potentials)	4	<u>L1</u>

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<u>L4</u>	L3 and doped and undoped	6	<u>L4</u>
<u>L3</u>	L1 and polysilicon and metallization	41	<u>L3</u>
<u>L2</u>	L1 and polysilicon a	6254293	<u>L2</u>
<u>L1</u>	((via or contact or hole) near4 lining)	4374	<u>L1</u>

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L4: Entry 1 of 6

File: USPT

Apr 9, 2002

US-PAT-NO: 6369430

DOCUMENT-IDENTIFIER: US 6369430 B1

TITLE: Method of preventing two neighboring contacts from a short-circuit caused by a void between them and device having the same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 2. Document ID: US 6171952 B1

L4: Entry 2 of 6

File: USPT

Jan 9, 2001

US-PAT-NO: 6171952

DOCUMENT-IDENTIFIER: US 6171952 B1

TITLE: Methods of forming metallization layers and integrated circuits containing such

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 3. Document ID: US 6090636 A

L4: Entry 3 of 6

File: USPT

Jul 18, 2000

US-PAT-NO: 6090636

DOCUMENT-IDENTIFIER: US 6090636 A

TITLE: Integrated circuits using optical waveguide interconnects formed through a semiconductor wafer and methods for forming same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 4. Document ID: US 5994215 A

L4: Entry 4 of 6

File: USPT

Nov 30, 1999

US-PAT-NO: 5994215

DOCUMENT-IDENTIFIER: US 5994215 A

TITLE: Method for suppression pattern distortion associated with
BPSG reflow

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 5. Document ID: US 5895261 A

L4: Entry 5 of 6

File: USPT

Apr 20, 1999

US-PAT-NO: 5895261

DOCUMENT-IDENTIFIER: US 5895261 A

TITLE: Process for making integrated circuit structure comprising
local area interconnects formed over semiconductor substrate by
selective deposition on seed layer in patterned trench

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 6. Document ID: US 5670425 A

L4: Entry 6 of 6

File: USPT

Sep 23, 1997

US-PAT-NO: 5670425

DOCUMENT-IDENTIFIER: US 5670425 A

TITLE: Process for making integrated circuit structure comprising
local area interconnects formed over semiconductor substrate by
selective deposition on seed layer in patterned trench

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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